PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No. : 09/933,468 Applicant : Christopher S. MacLellan Filed : August 20, 2001 T.C./A.U. : 2138 Examiner : John J. Tabone, Jr. Docket No. : EMC-01-018 Customer No. : 24227	Confirmation No.: 5620

Certificate of Mailing or Transmission 37 C.F.R. § 1.8

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11/6/06 Linda Valanzola

Date *Signature*

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

DECLARATION UNDER 37 C.F.R. §1.131

1. I, Christopher S. MacLellan, am the inventor of the above-referenced U.S. Patent Application No. 09/933,468 entitled "Testing System and Method of Using Same."

2. Prior to September 14, 2000, I conceived of, and reduced to practice, the invention described and claimed in U. S. Patent Application No. 09/933,468, as evidenced by source code, portions of which being attached hereto as Exhibits A-D.

3. Exhibit A is a directory listing of a UNIX file server containing the source code files for the invention as described in the patent application. The purpose of this exhibit is to establish that the invention was conceived of on or before September 14, 2000, as this is the last date the file was modified.

2. Exhibit B is a portion of code from a file A20SVC.v, with an electronic timestamp of September 14, 2000 as evidenced on line 2 of Exhibit A. The line numbers indicated in Exhibit B reference the line numbers of the original file A20SVC.v in its entirety. The entire file is not reproduced in this exhibit due to intellectual property contained within the file not pertaining to the patent application in question. This is the same file referenced in Exhibit A of my first affidavit dated June 12, 2006.

3. Exhibit C is a portion of code from a file A20CORE.v, with an electronic timestamp of September 14, 2000 as evidenced on line 1 of Exhibit A. The line numbers indicated in Exhibit C reference the line numbers of the original file A20CORE.v in its entirety. The entire file is not reproduced in this exhibit due to intellectual property contained within the file not pertaining to the patent application in question.

4. Exhibit D is a portion of code from a file A20UI.v, with an electronic timestamp of September 14, 2000 as evidenced on line 3 of Exhibit A. The line numbers indicated in Exhibit D reference the line numbers of the original file A20UI.v in its entirety. The entire file is not reproduced in this exhibit due to intellectual property contained within the file not pertaining to the patent application in question.

5. Referring to lines 33, 61, 89, 117, 122, 127, 132, and 137 of A20SVC.v, as shown in Exhibit B, there are multiple signals named "DIAGA", "DIAGB", "DIAGC", "DIAGD", "DIAGW", "DIAGX", "DIAGY", and "DIAGZ", respectively. The purpose of these signals, among other things, is to provide the control of the third logic section as claimed in applicant's Claim 1. By way of example, I will demonstrate how one of these signals flows through the source code and ultimately implements the method and apparatus recited in the claims. With

reference to the claims of the application, Exhibit B establishes the first logic section that may transmit one or more test-related signals for use during a test mode of the SUT.

6. Referring to Exhibit C, lines 421 and 576 establish, to someone skilled in the Verilog HDL language, that the 46-bit signal "DIAGAS" is connected to signal "DIAG" inside the A20UI instance "UIA". Similarly, lines 1521 and 1548 establish that the same 46-bit signal "DIAGAS" is also connected to signal "DIAGA" inside the A20SVC instance "SVC". Thus, signal "DIAGA" inside the A20SVC design (Exhibit B) is directly connected to signal "DIAG" inside the A20UI design (Exhibit D).

7. Referring now to Exhibit D, lines 361, 366, 368, and 370 connects bits 45, 10, 8, and 6 of signal "DIAG" to signals "DEN", "FUWDH", "FWOH", and "FWUH", respectively. Further, bits 10, 8, and 6 of "DIAG" only get coupled to their respective signals if bit 45 of signal "DIAG" was set to be a logic 1. Further inspection of file A20SVC by someone skilled in the Verilog HDL language would reveal that bits 45, 10, 8, and 6 of signal "DIAG" are independently settable by external sources, e.g. software algorithms from an external microprocessor, and are thus selectable.

8. Also referring to Exhibit D, lines 419 through 423 comprise a single logical expression, which is an example of a third logic section as claimed in the patent application. Upon inspection of both the logical expressions and the commentary accompanying each line of the file (comments are demarked with a "//" character sequence), the following can be observed: (i) signal "DATHV" is the intended, normal operating mode of the equation, and is passed to this third logic section from the second logic section as described in the applicant's claims; (ii) signals "FWUH", "FWUDH", and "FWOH" together comprise control signals passed to the third logic section from the first logic section; (iii) signals "CMDWR", "USEQ", "UACP6", "UREQ0", and "DATHVD" together comprise control signals external to the SUT. Taking lines 419 through 423 together as a single expression, it demonstrates "a third logic section that selectively couples the first logic section or the second logic section to the SUT based upon respective states of two control signals, one of the two control signals being transmitted to the third logic section from a source that is external to the SUT, the first logic section, the second

logic section, and the third logic section, the other of the two control signals being transmitted to the third logic section from the first logic section." Furthermore, based on the foregoing, "when the third logic section couples the first logic section to the SUT, the first logic section transmits the one or more test-related signals to the SUT, and when the third logic section couples the second logic section to the SUT, the second logic section transmits the one or more other signals to the SUT," as recited in claim 1.

9. Based on the foregoing description of the code, applicant asserts that the system embodied by the code and recited in claim 1 has been thoroughly tested to confirm that it works for its intended purpose and that the system is currently included in products sold by the assignee of the present patent application.

10. All of the statements made herein of my own knowledge are true and all statements made on information and belief are believed to be true. These statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment or both, under § 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application and any patent issuing thereon.

11-3-2006
Date of Signature

By: Christopher S. MacLellan
Christopher S. MacLellan

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Exhibit A

Line #	Text						
1	-rw-r--r--	1	chrismac	symmem	40270	Sep 14	2000 A20CORE.v
2	-rw-r--r--	1	chrismac	symmem	101745	Sep 14	2000 A20SVC.v
3	-rw-r--r--	1	chrismac	symmem	44550	Sep 14	2000 A20UI.v

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Exhibit B

Line #	Text	
33	DIAGA,	// 46-bit Diagnostic mode register to UI
61	DIAGB,	// 46-bit Diagnostic mode register to UI
89	DIAGC,	// 46-bit Diagnostic mode register to UI
117	DIAGD,	// 46-bit Diagnostic mode register to UI
122	DIAGW,	// 10-bit Diagnostic mode register to LI
127	DIAGX,	// 10-bit Diagnostic mode register to LI
132	DIAGY,	// 10-bit Diagnostic mode register to LI
137	DIAGZ,	// 10-bit Diagnostic mode register to LI

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Exhibit C

Line #	Text
421	A20UI UIA (.CLOCK(CLOCK),
576	.DIAG(DIAGAS[45:0]),
1521	A20SVC SVC (.CLOCK(CLOCK),
1548	.DIAGA(DIAGAS[45:0]),

Exhibit D

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Line #      Text
361         wire        DEN     = DIAG[45];       // Diagnostic Enabled
366         wire        FUWDH   = DEN & DIAG[10]; // Force Unexpected Write Data High
368         wire        FWOH    = DEN & DIAG[8]; // Force Write Overrun High
370         wire        FWUH    = DEN & DIAG[6]; // Force Write Underrun High
419         // Conditioned signals to allow diagnostic error forcing
420         assign DATHVI = ~FWUH & // If enabled, truncate DATHV to simulate underrun
421                 (DATHV | // Non-error case
422                 FUWDH & ~CMDWR & ((USEQ == UACP6) | (USEQ == UREQ0)) | // If enabled, force DATHV during
READ in states UACP6,UREQ0
423                 FWOH & DATHVD); // If enabled, extend DATHV by 1 clock to simulate overrun
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